REMARKS

In section 2 of the Office Action, the Examiner rejected claims 15-38 under 35 U.S.C. §102(e) as being anticipated by the Pal patent.

The Pal patent shows a prior art multicarrier transmitter 10 in Figure 1A. The multicarrier transmitter 10 receives serial input data at a rate Mf_s bits/sec, and the serial input data is grouped by a serial-to-parallel converter 12 into blocks of M bits at a symbol rate of f_s bits/sec. The modulators 14 modulate the serial input data groups onto N_c carriers that are spaced Δf_c apart. The modulated signals are then summed by an adder 16 and transmitted. A receiver demodulates the received signal by each of the N_c carriers, and m_n bits are recovered from each carrier.

Figure 1B of the Pal patent is a block diagram of a prior art multicarrier modulation system 100. The transmitter side of the multicarrier modulation system 100 includes an encoder 102 that encodes the digital signals. An IFFT unit 104 modulates the encoded signals onto multiple carriers. The modulated signals are converted to analog signals by a digital-to-analog

converter 106, and the analog signals are transmitted to a receiver over a channel 108.

In the receiver side of the multicarrier modulation system 100, the received analog signals are converted into digital signals by an analog-to-digital converter 110. The digital signals are supplied to a time domain equalizer (TEQ) 112 that compensates for attenuation and delay in each of the subchannels. The time domain equalized signals are converted from the time domain to the frequency domain by a FFT 114. The frequency domain signals are supplied to a frequency domain equalizer (FEQ) 116 that compensates for attenuation and delay in each of the subchannels. In effect, the FFT unit 114 and the frequency domain equalizer 116 operate to demodulate the digital signals from the multiple carriers. The demodulated signals are decoded by a decoder 118 to recover the data.

The Pal patent states that the operation of the time domain equalizer 112 is computationally complex and is not able to perfectly equalize the attenuation and delay in the channel response. Therefore, time domain equalization is typically performed by an adaptive equalization technique. Although adaptive equalization has been somewhat effective, the Pal patent states that

convergence of the adaptive equalizer is occasionally difficult to obtain. The Pal patent further states that the time domain equalization shown in Figure 1B utilizes a single equalization path and often has difficulty obtaining convergence.

The Pal patent, therefore, discloses parallel finite impulse response (FIR) filters that are used as a poly-path time domain equalizer (TEQ) to improve both the convergence and the effectiveness of time domain equalization. Because plural paths are provided through the time-domain equalizer, the receiver effectively receives the transmitted data over a plurality of channels. Each channel is modeled (Figure 4) as a tapped delay line implemented as a corresponding finite impulse response (FIR) filter whose filter tap coefficients are determined in dependence on one another.

Figure 2 of the Pal patent is a block diagram of a portion of a receiver 200 of a multicarrier, poly-path time domain equalizer modulation system. The receiver 200 receives analog signals from the channel 108 and supplies the analog signals to an analog-to-digital converter (ADC) 202. The ADC 202 oversamples the received analog signals by a factor of two. Hence, if

the analog signals are received at a rate R, the digital signals are output from the ADC 202 at a rate of 2R.

The digital signals from the ADC 202 are demultiplexed by a demultiplexer 204. The demultiplexer 204 forwards alternate ones of the digital signals to either a first effective channel or a second effective channel. The first effective channel includes a delay element 206 and a first time domain equalizer 208. The second effective channel includes a second time domain equalizer 210. The delay element 206 compensates for the delay induced on the second effective channel by the demultiplexer 204. An adder 212 combines respective equalized signals from the first and the second time domain equalizers 208 and 210. The output of the adder 212 is then supplied to the FFT unit 114 and subsequent portions of the receiver 100 such as illustrated in FIG. 1B.

Figure 3 shows a receiver 300 as an alternative embodiment. The receiver 300 receives analog signals from the channel 108. The received analog signals are supplied to first and second effective channels. The first effective channel includes a first ADC 302, a delay unit 304, and a first time domain equalizer 306. The second effective channel includes a second ADC 308 and a

second time domain equalizer 310. The first ADC 302 and the second ADC 308 sample the received analog signals at different phases. The delay unit 304 delays the first channel by the amount of the phase offset so that the respective sampled values of the first and second channels are in phase. The equalized signals produced by the first time domain equalizer 306 and the second time domain equalizer 310 are combined by an adder 312. The output of the adder 310 is supplied to the FFT 114 and subsequent portions of the receiver 100 such as illustrated in FIG. 1B.

Figure 4 shows a receiver 400 according to still another alternative embodiment. The receiver 400 includes first and second channels like the embodiments illustrated in Figures 2 and 3, but produces first and second channels 402 and 404 using two different antennae positioned at different locations near or approximate to the receiver 400. The analog signals received over the first channel 402 are converted into digital signals by a first ADC 406. The resulting digital signals are supplied to a first time domain equalizer 408. The analog signals received over the second channel 404 are converted by a second ADC to digital signals. These resulting digital signals are supplied to a second time

domain equalizer 412. An adder 414 adds the equalized signals from the first and the second equalized time domain equalizers 408 and 412. The output from the adder 414 is supplied to the FFT 114 and subsequent portions of the receiver 100 such as illustrated in FIG. 1B.

In the embodiment of Figure 4, the channels 406 and 404 are modeled as FIR filters having predetermined number of taps. The first and second time domain equalizers 408 and 412 used to compensate for distortion on each of the channels are implemented as FIR filters having a predetermined number of taps. The filter taps for the first and second time domain equalizers 408 and 412 are determined such that the effective length of the overall channel appears substantially shortened.

Figure 5 shows a model 500 for a two-path time domain equalizer. Signals are effectively transmitted over first and second channels 502 and 504. The first channel 502 is modeled as a FIR filter h_A, and the second channel 504 is modeled as a FIR filter h_B. The distortion or noise associated with the first channel 502 is represented by Noise A which is summed at an adder 506 with the signals received from the reception side of the first channel 502. The output of the adder 506 effectively forms channel signals Y_A. The channel signals

Y_A represent the signals that a receiver would receive and undergo a channel shortening by a channel shortening arm 508 to produce a shortened channel FIR response Z_A. The channel shortening arm 508 has a transfer function W_A and is preferably implemented as a corresponding FIR filter.

The distortion or noise associated with the second channel 504 is represented by Noise B which is summed at an adder 510 with the signals received from the reception side of the second channel 504. The output of the adder 510 forms effective channel signals Y_B. The effective channel signals Y_B represent the signals that a receiver would receive and undergo a channel shortening by a channel shortening arm 512 to produce a shortened channel FIR response Z_B. The channel shortening arm 512 has a transfer function W_B and is preferably implemented as a corresponding FIR filter.

The shortened channels Z_A and Z_B are added by an adder 514 to produce the equalized signals.

Figure 6 shows poly-path time domain equalization processing 600 in flow chart form. The poly-path time domain equalization processing 600 receives analog signals that have been transmitted over an actual channel and forms multiple effective channels. For example, two channels may be formed. In each

channel, the received analog signals are converted to digital signals. The poly-path time domain equalization processing 600 effectively shortens the channel length by using the transfer functions of a FIR filter within the time domain equalizer for each respective channel. The resulting equalized signals from each of the channels are then combined, and the combined signals are demodulated and decoded.

The Pal patent states that the time domain equalizer can be placed in a transmitter instead of a receiver in order to reduce noise enhancement and to shift power requirements between transmitter-receiver pairs. This time domain equalizer may be a single path time domain equalizer or a poly-path time domain equalizer.

Accordingly, Figure 9 shows a transmitter 900 that includes a time domain equalizer 902. The transmitter 900 includes the encoder 102 and the IFFT 104 of Figure 1B. The time domain signals produced by the IFFT unit 104 are supplied to the time domain equalizer 902. The time domain equalizer 902 reduces attenuation and phase distortion between carriers. The equalized signals output from the time domain equalizer 902 are supplied to a DAC 904, and the analog signals from the

DAC 904 are transmitted over the channel 108. The time domain equalizer 902 may be either a single path time domain equalizer or a poly-path time domain equalizer.

Figure 10 is a block diagram of a portion of a transmitter 1000 having a poly-path time domain equalizer. The transmitter 1000 includes the IFFT 104 that produces time domain signals that are supplied to first and second paths of the poly-path time domain equalizer. The first path includes a time domain equalizer 1002 and a delay unit 1004, and the second path includes a time domain equalizer 1006. The equalized signals from the first and second paths are supplied to a multiplexer 1008 whose output is oversampled by a DAC 1010. The multiplexer 1008 interleaves the signals from the first and second paths of the poly-path time domain equalizer. The analog signals produced by the DAC 1010 are transmitted over the channel 108.

Independent claim 15 is directed to a method of substantially eliminating all of the ghosts of a received main signal and reducing noise enhancement. The method comprises the following steps: a) processing the received main signal and the ghosts along n paths to produce n processed main signals and n processed ghosts, wherein each of the n paths includes a corresponding

finite filter, wherein the processing along each of the n paths does not substantially eliminate all of the ghosts, wherein n > 3, and wherein the processing along at least some of the n paths includes shifting data; and, b) adding the n processed main signals and the n processed ghosts such that, because of the addition of the n processed main signals and the n processed ghosts, all of the ghosts of the received main signal are substantially eliminated.

The time domain equalizers TEQ as disclosed in the Pal patent perform the function of shortening the channel. (See, for example, the Summary of the Invention in the Pal patent.) By shortening the channel, the time domain equalizers TEQ eliminate the ghosts that are far from the main signal. Thus, the time domain equalizers TEQ do not eliminate the ghosts that are closer to the main signal. Accordingly, the adders 212, 312, and 414 disclosed in the Pal patent do not add the processed main signals and ghosts such that, because of the addition, all of the ghosts of the received main signal are substantially eliminated as required by independent claim 15.

Therefore, for this reason, the Pal patent does not anticipate independent claim 15.

Moreover, the Pal patent shows only two processing paths in drawings. Therefore, in the drawings, n is not greater than 3 as required by independent claim 15.

In the text, the Pal patent does state at column 8, lines 50-53 that the poly-path time domain equalizer in the embodiment of Figure 4 can have two or more paths or channels modeled as corresponding FIR filters having predetermined numbers of taps. However, the poly-path time domain equalizer of Figure 4 has no delays in any of the paths.

Therefore, the Pal patent does not disclose a poly-path time domain equalizer having more than three paths in which at least some of the n paths includes data shifting.

The Examiner asserts that the Pal patent inherently discloses a poly-path time domain equalizer having more than three paths in which at least some of the n paths includes data shifting. However, this assertion is not correct.

The Pal patent discloses, in connection with Figure 2, a delay 206 that compensates for the delay imposed by the multiplexer 206 on the data in one path relative to the data in the other path. The Pal patent

does not suggest that the embodiment of Figure 2 can include additional paths, and the Pal patent does not suggest what sort of delays should be provided if additional paths were added to the embodiment of Figure 2.

The Pal patent discloses, in connection with Figure 3, a delay 304 that compensates for the phase offset between the ADCs 302 and 308. The Pal patent does not suggest that the embodiment of Figure 3 can include additional paths, and the Pal patent does not suggest what sort of delays should be provided if additional paths were added to the embodiment of Figure 3.

As discussed above, the embodiment of Figure 4 is the only embodiment where the Pal patent does suggest more than two paths. However, the embodiment of Figure 4 does not use a multiplexer and, therefore, no delay is required as in the case of the Figure 2 embodiment. Moreover, although the embodiment of Figure 4 does include an ADC in each of the paths, the phases of the ADCs are not offset with respect to one another as in the case of the Figure 3 embodiment. Therefore, no delay is required in the embodiment of Figure 4 to compensates for a phase offset between the ADCs 406 and 410.

Consequently, because the Pal patent does not suggest the use of delays in the only embodiment that can have more than two paths as disclosed by the Pal patent, processing along more than three paths some of which include data shifting is not inherently disclosed by the Pal patent.

For all of these additional reasons, the Pal patent does not anticipate independent claim 15.

Independent claim 26 is directed to an equalizer for processing blocks of data comprising n processing paths, n - 1 data shifters, n finite filters, and an adder. The n processing paths are arranged to process the blocks of data. Each of the n - 1 data shifters is in a corresponding one of the n processing paths so that one of the n processing paths has no data shifter. Each of the n finite filters is in a corresponding one of the n processing paths, and each of the n finite filters applies a corresponding set of finite filter coefficients to the blocks of data. Ghosts of the blocks of data are not eliminated as a result of the application of the sets of finite filter coefficients corresponding to the n finite filters, and $n > 2$. The adder is arranged to add outputs from the n processing

paths such that the addition substantially eliminates all of the ghosts of the blocks of data.

As discussed above, the time domain equalizers TEQ as disclosed in the Pal patent perform the function of shortening the channel. By shortening the channel, the time domain equalizers TEQ eliminate the ghosts that are far from the main signal. Thus, the time domain equalizers TEQ do not eliminate the ghosts that are closer to the main signal. Accordingly, the adders 212, 312, and 414 disclosed in the Pal patent do not add the processed main signals and ghosts such that, because of the addition, all of the ghosts of the received main signal are substantially eliminated as required by independent claim 26.

Therefore, for this reason, the Pal patent does not anticipate independent claim 26.

Moreover, the Pal patent shows only two processing paths in drawings. Therefore, in the drawings, n is not greater than 2 as required by independent claim 26.

In the text, the Pal patent does state at column 8, lines 50-53 that the poly-path time domain equalizer in the embodiment of Figure 4 can have two or more paths or channels modeled as corresponding FIR

filters having predetermined numbers of taps. However, the poly-path time domain equalizer of Figure 4 has no delays in any of the paths.

Therefore, the Pal patent does not disclose a poly-path time domain equalizer having more than two paths in which at least two of the paths includes data shifting.

The Examiner asserts that the Pal patent inherently discloses a poly-path time domain equalizer having more than two paths in which at least two of the paths includes data shifting. However, this assertion is not correct.

The Pal patent discloses, in connection with Figure 2, a delay 206 that compensates for the delay imposed by the multiplexer 206 on the data in one path relative to the data in the other path. The Pal patent does not suggest that the embodiment of Figure 2 can include additional paths, and the Pal patent does not suggest what sort of delays should be provided if additional paths were added to the embodiment of Figure 2.

The Pal patent discloses, in connection with Figure 3, a delay 304 that compensates for the phase offset imposed between the ADCs 302 and 308. The Pal

patent does not suggest that the embodiment of Figure 3 can include additional paths, and the Pal patent does not suggest what sort of delays should be provided if additional paths were added to the embodiment of Figure 3.

As discussed above, the embodiment of Figure 4 is the only embodiment where the Pal patent does suggest more than two paths. However, the embodiment of Figure 4 does not use a multiplexer and, therefore, no delay is required as in the case of the Figure 2 embodiment. Moreover, although the embodiment of Figure 4 does include an ADC in each of the paths, the phases of the ADCs are not offset with respect to one another as in the case of the Figure 3 embodiment. Therefore, no delay is required in the embodiment of Figure 4 to compensates for a phase offset imposed by the ADCs 406 and 410.

Consequently, because the Pal patent does not suggest the use of delays in the only embodiment that can have more than two paths as disclosed by the Pal patent, processing along more than two paths at least two of which include data shifting is not inherently disclosed by the Pal patent.

For all of these additional reasons, the Pal patent does not anticipate independent claim 26.

Because independent claims 15 and 26 are not anticipated by the Pal patent, dependent claims 16-25 and 27-42 are likewise not anticipated by the Pal patent.

Moreover, dependent claims 16, 24, and 35 relate to down sampling. The Examiner asserts that down sampling is inherently disclosed by the Pal patent. To be inherently disclosed, down sampling must be an inevitable consequence of what is disclosed in the Pal patent. The Examiner has not shown that down sampling is an evitable consequence to what is disclosed in the Pal patent. Therefore, the Examiner has not made out a prima facie case of inherency that shifts the burden to applicants.

Accordingly, for this reason also, dependent claims 16, 24, and 35 are not anticipated by the Pal patent.

Dependent claims 17, 25, 27, and 34 relate to spectral transformation applied at specified points. The Examiner asserts that spectral transformation at the recited points is inherently disclosed by the Pal patent. To be inherently disclosed, spectral transformation at these points must be an inevitable consequence of what is disclosed in the Pal patent. The Examiner has not shown that spectral transformation at the recited points is an

evitable consequence to what is disclosed in the Pal patent. Therefore, the Examiner has not made out a prima facie case of inherency that shifts the burden to applicants.

Accordingly, for this reason also, dependent claims 17, 25, 27, and 34 are not anticipated by the Pal patent.

Dependent claims 18-23 and 28-33 relate to pre-processing of the received main signal and the ghost. The Examiner asserts that pre-processing of the received main signal and the ghost is inherently disclosed by the Pal patent. To be inherently disclosed, pre-processing of the received main signal and the ghost must be an inevitable consequence of what is disclosed in the Pal patent. The Examiner has not shown that pre-processing of the received main signal and the ghost is an evitable consequence to what is disclosed in the Pal patent. Therefore, the Examiner has not made out a prima facie case of inherency that shifts the burden to applicants.

Accordingly, for this reason also, dependent claims 18-23 and 28-33 are not anticipated by the Pal patent.

Dependent claims 36 and 37 specify that half of the n - 1 data shifters shifts data in the data blocks to

the left and that half of the n - 1 data shifters shifts the data in the data blocks to the right. The Examiner asserts that an equalizer having n - 1 data shifters in which half of the n - 1 data shifters shifts data in the data blocks to the left and half of the n - 1 data shifters shifts the data in the data blocks to the right is inherently disclosed by the Pal patent. To be inherently disclosed, an equalizer having n - 1 data shifters in which half of the n - 1 data shifters shifts data in the data blocks to the left and half of the n - 1 data shifters shifts the data in the data blocks to the right must be an inevitable consequence of what is disclosed in the Pal patent. The Examiner has not shown that an equalizer having n - 1 data shifters in which half of the n - 1 data shifters shifts data in the data blocks to the left and half of the n - 1 data shifters shifts the data in the data blocks to the right is an evitable consequence to what is disclosed in the Pal patent. Therefore, the Examiner has not made out a prima facie case of inherency that shifts the burden to applicants.

Accordingly, for this reason also, dependent claims 36 and 37 are not anticipated by the Pal patent.

Newly added dependent claims 39 and 41 recite that at least some of the data shifting involves data shifting by one sample. The Pal patent discloses delays to compensate for multiplexing delays or phase offsets between ADCs. However, the Pal patent does not disclose or suggest that these delays are by one sample.

Accordingly, dependent claims 39 and 41 are not anticipated by the Pal patent.

Newly added dependent claims 40 and 42 recite that data shifting includes shifting the data in at least one path by one sample to the left and shifting the data in another path by one sample to the right. The Pal patent discloses delays to compensate for multiplexing delays or phase offsets between ADCs. However, the Pal patent does not disclose or suggest that these delays are by one sample to the right and/or left.

Accordingly, dependent claims 40 and 42 are not anticipated by the Pal patent.

CONCLUSION

In view of the above, it is clear that the claims of the present application are patentable over the art applied by the Examiner. Accordingly, allowance of these claims and issuance of the above captioned patent application are respectfully requested.

Respectfully submitted,

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